1024-BIT BIPOLAR PROGRAMMABLE ROM (256x4 PROM)

N82S126
N82S129

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The N82S126 (Open Collector Outputs) and the N82S129 (Tri-State Outputs) are Bipolar 1024-Bit Read Only Memories, organized as 256 words by 4 bits per word. They are Field-Programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard N82S126 and N82S129 are supplied with all outputs at logical "0". Outputs are programmed to a logic "1" level at any specified address by fusing a Ni-Cr link matrix.

The N82S126 and N82S129 are fully TTL compatible, and include on-chip decoding and two chip enable inputs for ease of memory expansion. They feature either Open Collector, or Tri-State outputs for optimization of word expansion in bussed organizations.

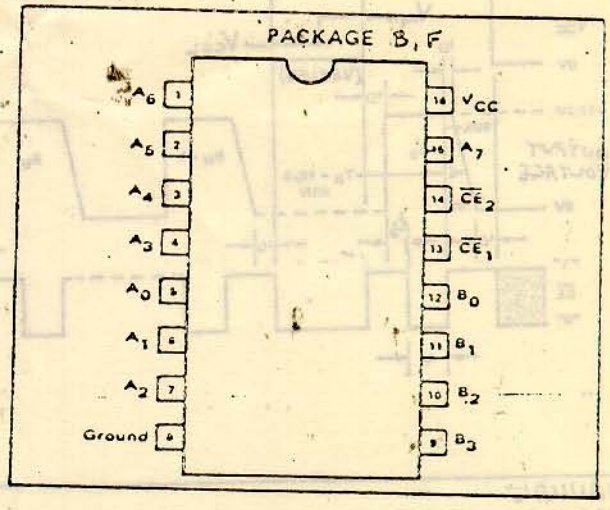
FEATURES

- ORGANIZATION - 256x4
- ADDRESS ACCESS TIME - 50ns, MAXIMUM
- POWER DISSIPATION -0.5mW/BIT, TYPICAL
- INPUT LOADING -(-100μA)MAXIMUM
- TWO CHIP ENABLE INPUTS
- ON-CHIP ADDRESS DECODING
- OUTPUT OPTION
  - TRI-STATE (N82S129)
  - OPEN COLLECTOR (N82S126)
- NO SEPARATE "FUSING" PINS
- UNPROGRAMMED OUTPUTS ARE "0" LEVEL

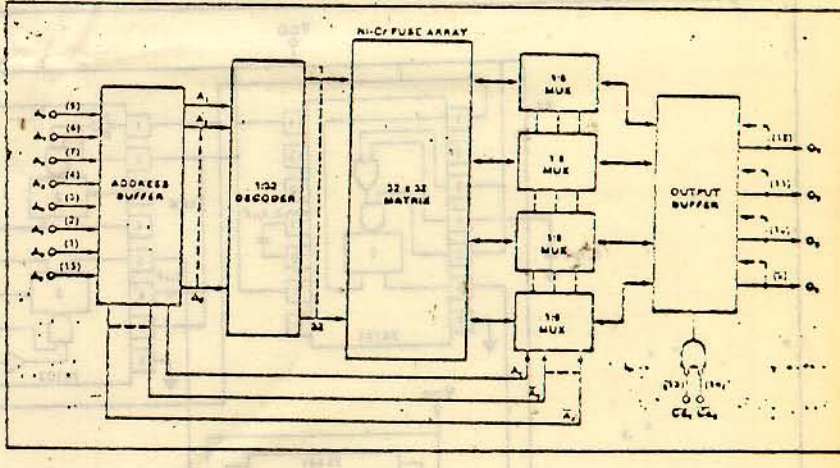
APPLICATIONS

- PROTOTYPING / VOLUME PRODUCTION
- SEQUENTIAL CONTROLLERS
- MICROPROGRAMMING
- HARDWIRED ALGORITHMS
- CONTROL STORE
- RANDOM LOGIC
- CODE CONVERSION

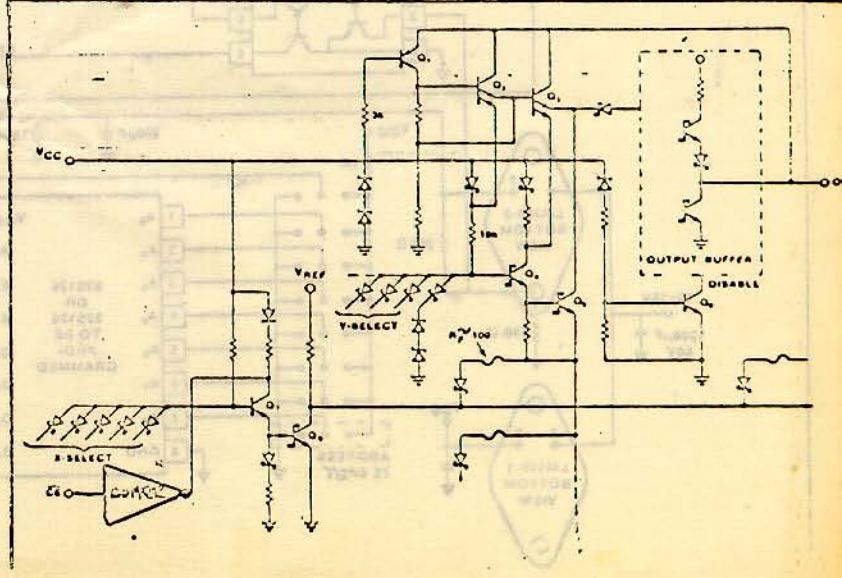
PIN CONFIGURATION.



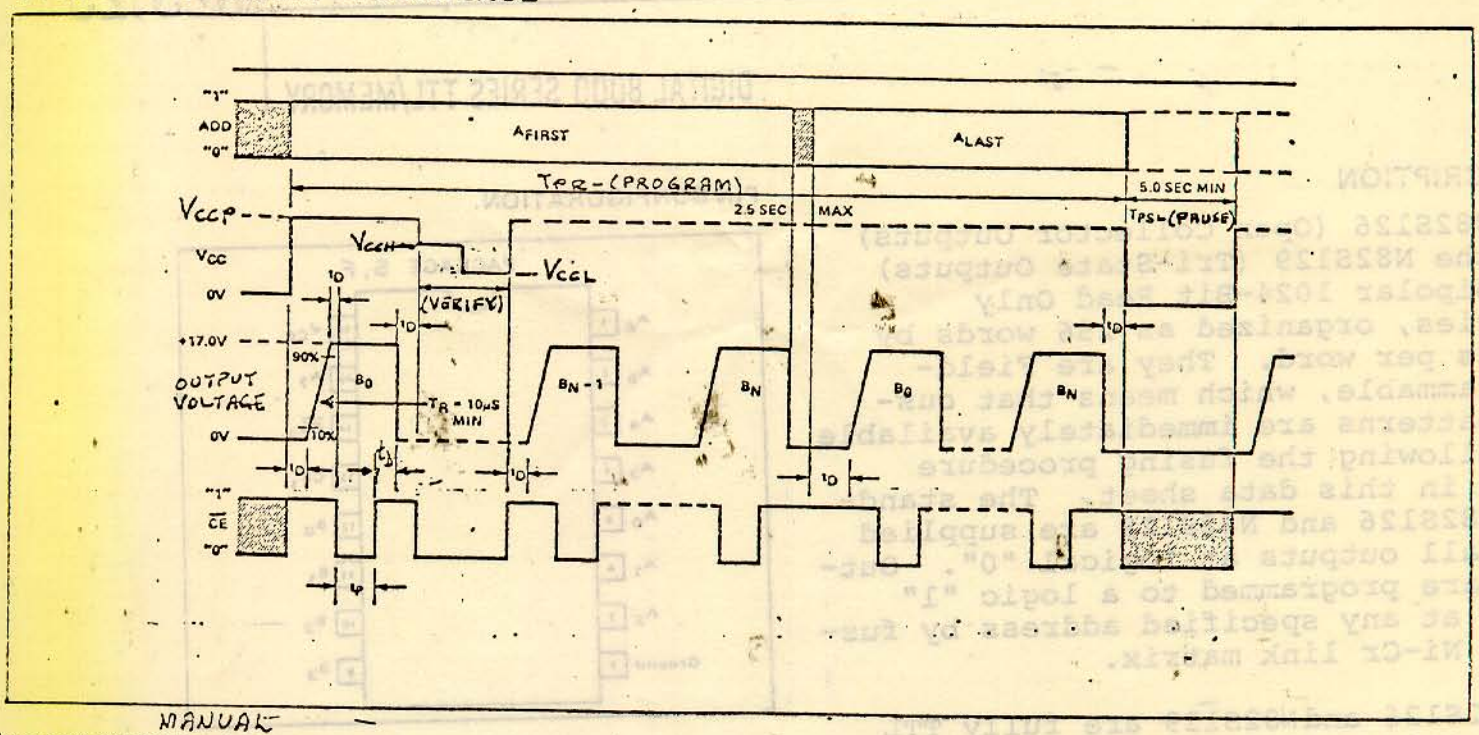
BLOCK DIAGRAM



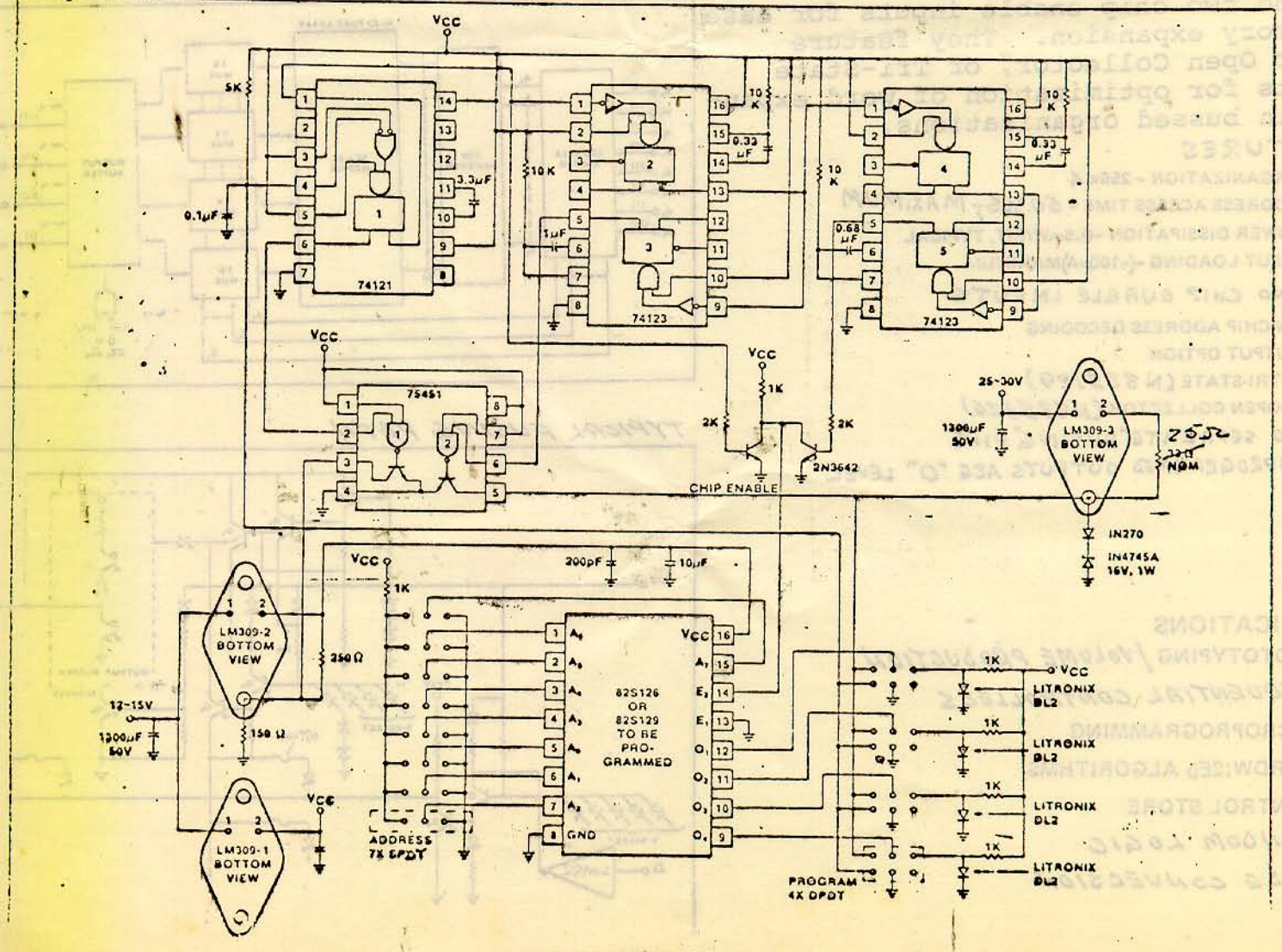
TYPICAL FUSING PATH



TYPICAL PROGRAMMING SEQUENCE



N82S126/129 MANUAL PROGRAMMER



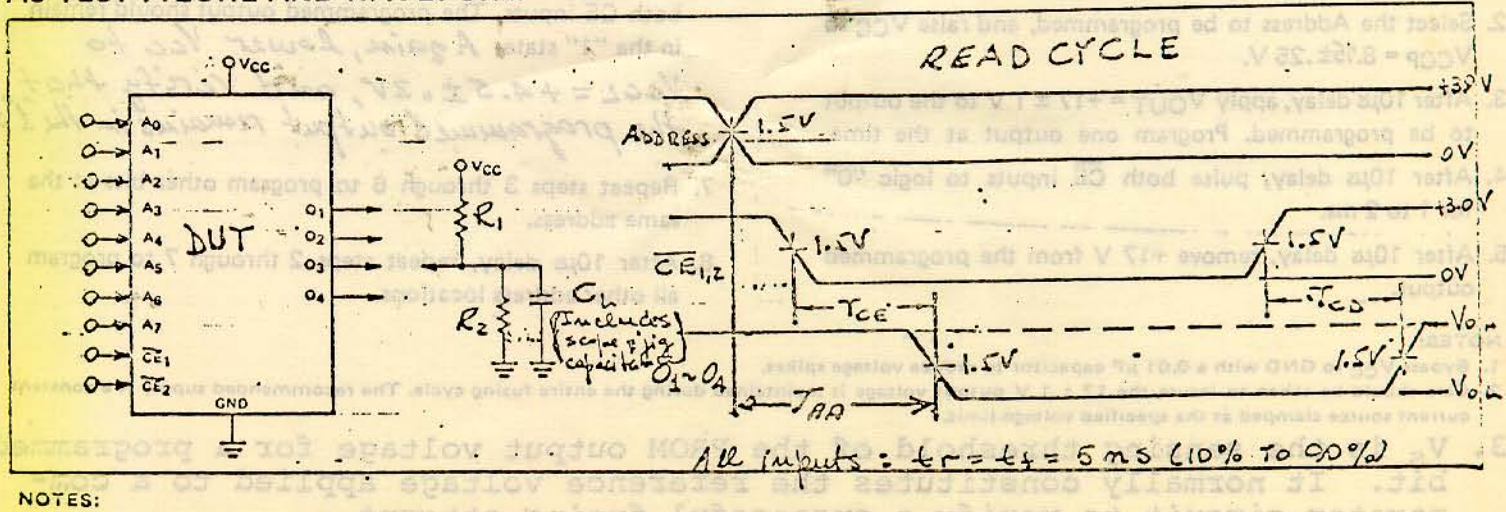
ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75\,V \leq V_{CC} \leq 5.25$

PARAMETER		TEST CONDITIONS[1]	LIMITS MIN	TYP[2]	MAX	UNIT
V_{OL}	"0" output voltage	I_{OUT} = 16mA			0.5	V
I_{OLK}	Output Leakage Current (N82S126)	$\overline{CE}_1$ or $\overline{CE}_2$ = "1", V_{OUT} = 5.5V			40	μA
$I_{O(off)}$	Hi-Z state Output Current (N82S129)	$\overline{CE}_1$ or $\overline{CE}_2$ = "1", V_{OUT} = 5.5 V			40	μA
		$\overline{CE}_1$ or $\overline{CE}_2$ = "1", V_{OUT} = 0.5			-40	μA
V_{OH}	"1" output voltage (N82S129)	$\overline{CE}_1$ or $\overline{CE}_2$ = "0", I_{OUT} = -2.4 mA, "1" Stored	2.4			V
I_{IL}	"0" input current	V_{IN} = 0.4 V			-100	μA
I_{IH}	"1" input current	V_{IN} = 5.5 V			40	μA
V_{IL}	"0" level input voltage				.85	V
V_{IH}	"1" level input voltage		2.0			V
I_{CC}	V_{CC} supply Current			105	120	mA
V_{IC}	Input clamp voltage	I_{IN} = -18 mA		-0.8	-1.2	V
I_{OS}	Output short circuit current (N82S129)	V_{OUT} = 0 volts	-20		-70	mA

SWITCHING CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP[2]	MAX	UNIT
PROPAGATION DELAY						
T_{AA}	Address to output	C_L = 30 pF		35	50	ns
T_{CD}	Chip disable to output	$R_1 = 270\,\Omega$		15	20	ns
T_{CE}	Chip enable to output	$R_2 = 600\,\Omega$		15	20	ns

AC TEST FIGURE AND WAVEFORM



NOTES:

1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, and T_A = +25°C.

PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device) — $T_A = +25°C$

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
POWER SUPPLY VOLTAGE						
V_{CCP}[1]	To program	I_{CCP} = 350 ± 50 mA (Transient or steady state)	8.5	8.75	9.0	V
V_{CCH}	Upper Verify Limit		5.3	5.5	5.7	V
V_{CCL}	Lower Verify Limit		4.3	4.5	4.7	V
V_S[2]	Verify Threshold		0.9	1.0	1.1	V
I_{CCP}	Programming supply current	V_{CCP} = +8.75 ± .25 V	300	350	400	mA
INPUT VOLTAGE						
V_{IH}	Logical "1"		2.4		5.5	V
V_{IL}	Logical "0"		0	0.4	0.8	V
INPUT CURRENT						
I_{IH}	Logical "1"	V_{IH} = +5.5V			50	μA
I_{IL}	Logical "0"	V_{IL} = +0.4V			-500	μA
V_{OUT}[2]	Output programming voltage	I_{OUT} = 200 ± 20 mA (Transient or steady state)	16.0	17.0	18.0	V
I_{OUT}	Output programming current	V_{OUT} = +17 ± 1 V	180	200	220	mA
T_R	Output pulse rise time		10		50	μs
t_P	$\overline{CE}$ programming pulse width		1		2	ms
t_D	Pulse sequence delay		10			μs
T_{PR}	Programming time	$V_{CC} = V_{CCP}$			2.5	sec
T_{PS}	Programming pause	V_{CC} = 0 V	5			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$[4]	Programming duty cycle				33	%

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC}.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP} = 8.75±.25 V.
3. After 10μs delay, apply V_{OUT} = +17 ± 1 V to the output to be programmed. Program one output at the time.
4. After 10μs delay, pulse both $\overline{CE}$ inputs to logic "0" for 1 to 2 ms.
5. After 10μs delay, remove +17 V from the programmed output.
6. To verify programming, after 10μs delay, lower V_{CC} to V_{CCH} = +5.5 ± .2V, and apply a logic "0" level to both $\overline{CE}$ inputs. The programmed output should remain in the "1" state. Again, lower V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the "1" state.
7. Repeat steps 3 through 6 to program other bits at the same address.
8. After 10μs delay, repeat steps 2 through 7 to program all other address locations.

NOTES:

1. Bypass V_{CC} to GND with a 0.01 μF capacitor to reduce voltage spikes.
2. Care should be taken to insure the 17 ± 1 V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.

3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.

4. Continuous fusing for an unlimited time is also allowed, provided that